Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] 1.A method for making an asymmetric interior structure in a trench or contact hole of a substrate layer, comprising the steps of:
forming at least one trench or contact hole in a substrate layer, the trench or contact opening comprising a first sidewall, second sidewall, and a bottom;
forming a first dielectric layer on the first sidewall, the second sidewall, and the bottom;
performing a title angle ion implantation process to dope ions into the first dielectric layer on the first sidewall and on the bottom, but not dope ions into the first dielectric layer on the second sidewall, thereby resulting in etching selectivity between the doped first dielectric layer on the first sidewall and on the bottom, and the non-doped first dielectric layer on the second sidewall; and
selectively etching away the doped first dielectric layer on the first sidewall and on the bottom, thereby forming an asymmetric interior structure in the trench or contact hole.

[c2] 2.The method of claim 1 wherein the first dielectric layer is a silicon oxide layer.

[c3] 3The method of claim 1 wherein the first dielectric layer is a silicon nitride layer.

[c4] 4.A method for making an asymmetric interior structure in a trench or contact hole of a substrate layer, comprising the steps of:
forming at least one trench or contact hole in a substrate layer, the trench or contact opening comprising a first sidewall, second sidewall, and a bottom
forming a first dielectric layer on the first sidewall, the second sidewall, and the bottom;
performing a title angle ion implantation process to dope ions into the first dielectric layer on the first sidewall and on the bottom, but not dope ions into the first dielectric layer on the second sidewall, thereby resulting in etching selectivity between the doped first dielectric layer on the first sidewall and on the bottom, and the non-doped first dielectric layer on the second sidewall;
selectively etching away the doped first dielectric layer on the first sidewall and on the bottom;
growing a second dielectric layer on the exposed second sidewall and the bottom; and
selectively etching away the first dielectric layer.

[c5] 5.The method of claim 4 wherein the first dielectric layer is a silicon oxide layer, and the second dielectric layer is

an RTN silicon nitride layer.

[c6] 6.The method of claim 4 wherein the first dielectric layer is a silicon nitride layer, and the second dielectric layer is an RTO silicon oxide layer.